UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
HOLDER, ANNER N

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>15 September 2008</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,2,4-9,11-15 and 17-20</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,2,4-9,11-15 and 17-20</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>01 April 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.　　Applicant's arguments with respect to claims 1-2, 4-9, 11-15, and 17-20 have been considered but are moot in view of the new ground(s) of rejection.

2.　　As to Applicant's arguments regarding Kim, pg. 11 concerning "comprises one or more bits, each of which are associated with a corresponding one or more motion vector registers, wherein the one or more bits are in a particular stat, based on whether the corresponding motion vector register stores a motion vector." Kim discloses 8 bit number in the residual value. [col. 5 line 57- col. 6 lines 20]

Claim Rejections - 35 USC § 103

3.　　The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.　　Claims 1, 2, 4, 8-9, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise et al. (Wise) US 2003/0156652 A1 in view of Abelard et al. US 7,130,526 B2 further in view of Kato US 5,701,164.

5.　　As to claim 1, Wise teaches a circuit for determining addresses for reference pixels, said circuit comprising: an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; [Pg. 51 ¶ 0682 Table A.3.2] and logic for determining whether the parameters received by the input are

valid, [Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236]

Wise does not explicitly the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input.

Abelard teaches the logic determines whether the parameters received by the input are valid based on the picture type indicator received by the input. [col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

It would have been obvious at the time the invention was made to incorporate the teachings of Abelard with device of wise allowing for improved coding and reproduction.

Wise (modified by Abelard) does not explicitly teach the logic determines whether the parameters received by the input are valid based on the number of motion vectors received by the input.

Kato teaches counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Wise (modified by Abelard) allowing for improved coding.

6.   As to claim 2, Wise (modified by Abelard and Kato) teaches an arithmetic logic unit for calculating one or more addresses depending on whether the logic determines that the addresses are valid. [Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236].

7.   As to claim 4, Wise (modified by Abelard and Kato) teaches a control register for providing the type of pictures and indicating the number of motion vectors received to the logic. [Wise - Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

8.   As to claim 8, Wise teaches receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; [Pg. 51 ¶ 0682 Table A.3.2] and determining the validity of the parameters; [Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236] and calculating one or more addresses after determining the validity of the parameters, if the parameters are valid. [Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236]

Wise does not explicitly the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input.

Abelard teaches the logic determines whether the parameters received by the input are valid based on the picture type indicator received by the input. [col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

It would have been obvious at the time the invention was made to incorporate the teachings of Abelard with device of wise allowing for improved coding and reproduction.

Wise (modified by Abelard) does not explicitly teach the logic determines whether the parameters received by the input are valid based on the number of motion vectors received by the input.

Kato teaches counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Wise (modified by Abelard) allowing for improved coding.

9.   As to claim 9, Wise (modified by Abelard and Kato) teaches fetching pixels from the one or more addresses after determining the validity of the parameters, if the parameters are valid. [Pg. 163 ¶ 2587]

10.   As to claim 11, Wise (modified by Abelard and Kato) teaches determining the validity of the parameters further comprises determining that the parameters are invalid if the type of picture is an I-picture and any motion vectors are received. [Wise- Pg. 51 ¶ 0682 Table A.3.2; Pg. ¶ 0160; Pg. 13 ¶ 0165; Pg. 18 ¶ 0220-0221; Pg. 117 ¶ 1595; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

11.   Claims 5-7, 12-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wise et al. (Wise) US 2003/0156652 A1 in view of Abelard et al. US 7,130,526 B2 further in view of Kato US 5,701,164 further in view of Kim et al. (Kim) US 6,215,823 B1.

12.   As to claim 5, Wise (modified by Abelard and Kato)) teaches one or more motion vector registers for storing motion vectors received by the input; [Wise - Pg. 51 ¶ 0682 Table A.3.2]

Wise (modified by Abelard and Kato) does not explicitly teach the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector.

Kim teaches the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector. [Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57- col. 6 lines 20]

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kim with the coding device of Wise (modified by Abelard and Kato) allowing for reduction of errors in image reproduction and the speed of decoding.

13.   As to claim 6, Wise (modified by Abelard, Kato and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state. [K Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57- col. 6 lines 20; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

14.   As to claim 7, Wise (modified by Abelard, Kato and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B- picture and less than two of the one or more bits are in the particular

state. [Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col.

23 lines 4-41; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 line 57-

col. 6 lines 20; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

15.   As to claim 12, Wise (modified by Abelard, Kato and Kim) teaches determining

the validity of the parameters further comprises determining that the parameters are

invalid if the control register indicates that the type of picture is a B-picture and less than

two of the one or more bits are in the particular state. [Wise- Pg. 51 ¶ 0682 Table A.3.2;

Pg. ¶ 0160; Pg. 13 ¶ 0165; Pg. 18 ¶ 0220-0221; Pg. 117 ¶ 1595; Kim - Abstract; Col. 1

Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Kato - abstract; fig. 2; fig. 6; col. 19

line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Abelard - col. 2 lines 50-56;

col. 4 lines 25-34, 49-58]

16.   As to claim 13, Wise teaches a video decoder for decoding macroblocks, said

video decoder comprising: a processor for decoding a set of parameters, [Abstract; Pg.

1 ¶ 0002] a picture type parameter indicating a type of picture; [Pg. 51 ¶ 0682 Table

A.3.2] a motion vector address computer for determining the validity of the set of

parameters, and calculating addresses associated with motion vectors if the set of

parameters are valid; [Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶

2073, ¶ 2079; Pg. 148 ¶ 2236] and a video request manager for fetching reference

pixels at the addresses calculated by the motion vector address computer, if the motion

vector address computer determines that the set of parameters are valid. [Pg. 31 ¶

0400; Pg. 163 ¶ 2587]

Wise does not specifically teach motion vectors indicating reference pixels associated with the macroblock and as to the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input, motion vectors indicating reference pixels associated with the macroblock.

Abelard teaches the logic determines whether the parameters received by the input are valid based on the picture type indicator received by the input. [col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

It would have been obvious at the time the invention was made to incorporate the teachings of Abelard with device of wise allowing for improved coding and reproduction.

Wise (modified by Abelard) does not explicitly teach the logic determines whether the parameters received by the input are valid based on the number of motion vectors received by the input.

Kato teaches counting the number of motion vectors received by the input. [abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kato with the device of Wise (modified by Abelard) allowing for improved coding.

Wise (modified by Abelard and Kato) is silent as to motion vectors indicating reference pixels associated with the macroblock.

Kim teaches motion vectors indicating reference pixels associated with the macroblock. [Col. 1 Lines 44-57]

It would have been obvious to one of ordinary one of ordinary skill in the art to combine the teachings of Kim with the coding device of Wise (modified by Abelard and Kato) allowing for reduction of errors in image reproduction and the speed of decoding.

17.   As to claim 14, Wise (modified by Abelard, Kato and Kim) teaches the motion vector address computer further comprises: an input for receiving parameters, the parameters comprising a picture type indicator for indicating a type of a picture; [Wise - Pg. 51 ¶ 0682 Table A.3.2] and logic for determining whether the parameters received by the input are valid. [Kim - Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

18.   As to claim 15, (modified by Abelard, Kato and Kim) teaches the motion vector address computer further comprises: an arithmetic logic unit for calculating one or more addresses after the logic determines that the addresses are valid. [Wise - Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236]

19.   As to claim 16, (modified by Abelard, Kato and Kim) teaches the logic determines whether the parameters received by the input are valid based on the picture type indicator and the number of motion vectors received by the input. [Kim - Col. 1 Lines 44-57; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

20.   As to claim 17, (modified by Abelard, Kato and Kim) teaches the motion vector address computer further comprises: a control register for providing the type of pictures

[Wise - Pg. 51 ¶ 0682 Table A.3.2] and indicating the number of motion vectors received to the logic. [Wise - Fig. 23; Fig. 131; Fig. 127; Pg. 39 ¶ 0505, ¶ 0510; Pg. 142 ¶ 2073, ¶ 2079; Pg. 148 ¶ 2236; ;Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

21.   As to claim 18, Wise (modified by Abelard, Kato and Kim) teaches the motion vector address computer further comprises: one or more motion vector registers for storing motion vectors received by the input; [Wise - Pg. 51 ¶ 0682 Table A.3.2] and wherein the control register comprises one or more bits, each of which are associated with a corresponding one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector. [Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Kato - abstract; fig. 2; fig. 6; col. 19 line 48 col. 20 line 3; col. 20 lines 40-55; col. 23 lines 4-41]

22.   As to claim 19, Wise (modified by Abelard, Kato and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is an I-picture and any of the one or more bits are in the particular state. [Wise- Pg. 51 ¶ 0682 Table A.3.2; Pg. ¶ 0160; Pg. 13 ¶ 0165; Pg. 18 ¶ 0220-0221; Pg. 117 ¶ 1595; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

23.   As to claim 20, Wise (modified by Abelard, Kato and Kim) teaches the logic determines that the parameters are invalid if the control register indicates that the type of picture is a B-picture and less than two of the one or more bits are in the particular

state. [Wise- Pg. 51 ¶ 0682 Table A.3.2; Pg. ¶ 0160; Pg. 13 ¶ 0165; Pg. 18 ¶ 0220-0221; Pg. 117 ¶ 1595; Kim - Abstract; Col. 1 Lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; Abelard - col. 2 lines 50-56; col. 4 lines 25-34, 49-58]

Conclusion

24.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mihara US 6,163,573; Kawaharada et al. US 2004/0105589.

25.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANNER HOLDER whose telephone number is (571)270-1549. The examiner can normally be reached on M-Th, M-F 8 am - 3 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418.   The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.   Status information for published applications may be obtained from either Private PAIR or Public PAIR.   Status information for unpublished applications is available through Private PAIR only.   For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anner Holder/
Examiner, Art Unit 2621

/Tung Vo/

Primary Examiner, Art Unit 2621